Notice of Allowability	Application No.	Applicant(s)	
	10/740,034	HIRASE, YOSHIYA	
	Examiner	Art Unit	
	MENGYAO ZHE	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/12/2009*.

2. ☒ The allowed claim(s) is/are *1, 4-7, 10-13, 16-19, 21-22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Harry Smith on 3/27/2009.

Please amend the specification on Pg 5, lines 15-19 as follows:

i) Fill in the U.S. Patent Application No, on line 16 as 10/740,036

ii) Strike out the Attorney Docket No in the parentheses on lines 18-19.

The application has been amended as follows:

1. (Currently Amended) A device architecture comprising:

a processor arranged to run an operating system (OS) comprising an OS scheduler;

hardware comprising a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs); and

interposed between said OS and said DCHL layer, a TiEred Multi-media Acceleration Scheduler (TEMAS) that cooperates with the OS scheduler for scheduling the LEs of the DCHL to execute applications in accordance with inherited application priorities, where the TEMAS operates in response to configuration requests to configure and reconfigure at least some of the plurality of LEs using the inherited application priorities such that at one time a particular LE is scheduled for operation with a first algorithm logic, and at another time the same particular LE is scheduled for operation with a second, different algorithm logic, where the TEMAS is comprised of a Tier-1 scheduler that communicates with the OS scheduler to determine a difference in timing for the DCHL hardware and at least one Tier-2 scheduler interposed between the Tier-1 scheduler and one DCHL configurable device that operates in response to configuration requests from the Tier-1 scheduler.

2. Cancelled

3. Cancelled

4. (Original) A device architecture as in claim 1, where said plurality of LEs are disposed within at least one context plane.

5. (Currently Amended) A device architecture as in claim ~~2~~ 1, comprising an application layer that comprises at least one application, a service layer that comprises said Tier-1 scheduler and said OS scheduler, a node layer that comprises said at least one Tier-2 scheduler that is coupled to a scheduling algorithm of said Tier-1 scheduler, and a hardware layer that comprises said at least one DCHL configurable device.

6. (Original) A device architecture as in claim 1, where said device comprises a device having wireless communications capability.

7. (Currently Amended) A method comprising:

providing an operating system (OS) comprising an OS scheduler and a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs);

interposing between said OS and said DCHL layer a TiEred Multi-media Acceleration Scheduler (TEMAS); and

operating the TEMAS in cooperation with the OS scheduler for scheduling the LEs of the DCHL to execute applications in accordance with inherited application priorities, where operating the TEMAS comprises responding to configuration requests to configure and reconfigure at least some of the plurality of LEs using the inherited application priorities such that at one time a particular LE is scheduled for operation with a first algorithm logic, and at another time the same particular LE is scheduled for operation with a second, different algorithm logic, where the TEMAS is comprised of a Tier-1 scheduler that communicates with the OS scheduler to determine a difference in timing for the DCHL hardware and at least one Tier-2 scheduler interposed between the Tier-1 scheduler and one DCHL configurable device that operates in response to configuration requests from the Tier-1 scheduler.

8. Cancelled

9. Cancelled

10. (Original) A method as in claim 7, where said plurality of LEs are disposed within at least one context plane.

11. (Currently Amended) A method as in claim ~~8~~ 7, comprising an application layer that comprises at least one application, a service layer that comprises said Tier-1 scheduler and said OS scheduler, a node layer that comprises said at least one Tier-2 scheduler

that is coupled to a scheduling algorithm of said Tier-1 scheduler, and a hardware layer that comprises said at least one DCHL configurable device.

12. (Previously Presented) A method as in claim 7, executed in a device having wireless communications capability.

13. (Currently Amended) An apparatus, comprising:

an applications layer comprising a plurality of applications;

a processor arranged to run a service layer comprising an operating system (OS) having an OS scheduler;

hardware comprising a hardware layer comprising Dynamic Configurable Hardware Logic (DCHL) comprised of a plurality of Logic Elements (LEs); and

interposed between said OS and said DCHL in said service layer and in a node layer, a TiEred Multi-media Acceleration Scheduler (TEMAS) that cooperates with the OS scheduler for scheduling the LEs of the DCHL to execute said applications in accordance with inherited application priorities, where operating the TEMAS comprises responding to configuration requests to configure and reconfigure at least some of the plurality of LEs using the inherited application priorities such that at one time a particular LE is scheduled for operation with a first algorithm logic, and at another time the same particular LE is scheduled for operation with a second, different algorithm logic, where the TEMAS is comprised of a Tier-1 scheduler that communicates with the OS scheduler to determine a difference in timing for the DCHL hardware and at least one Tier-2 scheduler interposed between the Tier-1 scheduler and one DCHL configurable device that operates in response to configuration requests from the Tier-1 scheduler.

14. Cancelled

15. Cancelled

16. (Previously Presented) An apparatus as in claim 13, where said plurality of LEs are disposed within at least one context plane.

17. (Previously Presented) An apparatus as in claim 13, where said apparatus comprises a cellular telephone.

18. (Previously Presented) An apparatus as in claim 13, where said apparatus comprises a wireless communications device, and where said applications comprise multimedia applications.

19. (Currently Amended) An apparatus, comprising:

a plurality of hardware logic elements;

a logic element scheduler coupled to said plurality of hardware logic elements; and

an application scheduler coupled to said logic element scheduler and to an operating system scheduler, said application scheduler configured to receive information from said operating system scheduler comprising at least a scheduling order of applications and a priority of the applications and to generate and send application scheduling events to said logic element scheduler in accordance with said received information;

where said logic element scheduler responds to receipt of scheduling events to configure and reconfigure at least some of the plurality of hardware ~~logical~~ logic elements such that at one time a particular hardware logic element is scheduled for operation with a first algorithm logic for executing the first algorithm logic, and at another time the same particular hardware logic element is scheduled for operation with a second, different algorithm logic for executing the second, different algorithm logic, where said application scheduler is further configured to receive feedback of communication overhead from said logic element scheduler to use in adjusting scheduling timing for the hardware logic elements.

20. Cancelled

21. (Currently Amended) The apparatus of claim 19, where said logic element scheduler is further configured use the priority information when scheduling the application logics onto the hardware logic elements.

22. (Previously Presented) The apparatus of claim 19, embodied in a device having wireless communications capability.

REASONS FOR ALLOWANCE

3. The following is an examiner's statement of reasons for allowance:

All the independent claims contain the limitation of a two layered intermediate scheduler wherein the first layer communicates with the OS to determine the difference in timing for the hardware logic elements and the second layer interposed between the first layer and the hardware logic element that operates in response to configuration requests from the first layer.

All of the cited prior art at best teaches an intermediate scheduler that cooperates with another scheduler to configure a hardware. However, none of the prior art of record details the two layered structure of the intermediate scheduler where the first layer is specifically responsible for communicating with the OS scheduler to determine the difference in timing for the hardware. Therefore, the claims are allowable for at least those reasons.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193